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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BOKHARI, SYED M	
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2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/510,406	PORTER ET AL.	
	Examiner	Art Unit	
	Syed Bokhari	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/29/2004 and 10/05/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because of the total number of words used, exceeds the limit as described above. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-8, 11-12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (USP 5,062,124) in view of Eng et al. (USP 6,791,987 B1).

Hayashi et al. discloses a network synchronization system in a distributed communication system with the following features: regarding claim 1, over a network comprising plurality of modules interconnected via transmission links (Fig. 2,

synchronizing communication devices, see "distributed communication system" recited in column 3 lines 45-48), having a single input and one or more outputs (Fig. 4, node distribution, see "load input" recited in column 6 lines 18-22), where all the outputs are phase locked to each other but are not synchronized with respect to the input (Fig. 1, distributed communication system, see "synchronous communication system" recited in column 1 lines 34-47 in the Background of the invention), means for determining the accumulated phase difference between the input clock and the output clock of each module (Fig. 2, synchronizing communication devices, see "phase difference obtaining means" recited in column 3 lines 51-65), means for transmitting the accumulated phase difference to the terminating module in the network (Fig. 3, distributed network, see "transmission of phase difference" recited in column 5 lines 13-19), and means for utilizing the received accumulated phase difference at the terminating module to lock the output clock at the terminating module to the input clock at the source module (Fig. 2, synchronizing communication devices, see "synchronizing with the reference clock" recited in column 3 lines 51-65 and column 8 lines 2-7); regarding claim 2, in which the accumulated phase difference is transmitted at regular intervals (Fig. 1, distributed communication system, see "phase difference information" recited in column 4 lines 51-58); regarding claim 3, the determining means comprises a first counter for counting clock cycles of the input signal clock (Fig. 5, communication device, see "counter 43" recited in column 7 lines 10-16), a second counter for counting cycles of the output signal clock (Fig. 5, communication device, see "counter 43" recited in column 7 lines 17-25), and means for simultaneously reading the counts of the first and

second counters (Fig. 5, communication devices 11 and 12, see "selector 102" recited in column 8 lines 17-22 and lines 39-43); regarding claim 4, comprising a latch for storing the count of the counter counting the higher frequency clock (Fig.4, node distribution, see "latch for store" recited in column 6 lines 30-33) and the count being clocked into the latch by an edge of the lower frequency clock (Fig.4, node distribution, see "latch for store" recited in column 6 lines 36-39); regarding claim 6, the network comprising a plurality of modules interconnected via transmission links (Fig. 2, synchronizing communication devices, see "distributed communication system" recited in column 3 lines 45-48), and having a single input and one or more outputs (Fig. 4, node distribution, see "load input" recited in column 6 lines 18-22), where all the outputs are phase locked to each other but are not synchronized with respect to the input (Fig. 1, distributed communication system, see "synchronous communication system" recited in column 1 lines 34-47 in the Background of the invention), the method comprising the steps of determining the accumulated phase difference between the input clock and the output clock at each module (Fig. 2, synchronizing communication devices, see "phase difference obtaining means" recited in column 3 lines 51-65), transmitting the determined accumulated phase difference to the terminating module (Fig. 3, distributed network, see "transmission of phase difference" recited in column 5 lines 13-19), and utilizing the received accumulated phase difference at the terminating network to recover the clock at the source module of the network (Fig. 2, synchronizing communication devices, see "synchronizing with the reference clock" recited in column 3 lines 51-65 and column 8 lines 2-7); regarding claim 7, the accumulated phase

difference is transmitted (Fig. 1, distributed communication system, see "phase difference information" recited in column 4 lines 51-58); regarding claim 8, applying the input clock of a module to a first counter within the module (Fig. 5, communication device, see "counter 43" recited in column 7 lines 10-16), applying the output clock of the module to a second counter within the module (Fig. 5, communication device, see "counter 43" recited in column 7 lines 17-25) and reading the counts of the first and second counters simultaneously at given intervals (Fig. 5, communication devices 11 and 12, see "selector 102" recited in column 8 lines 17-22 and lines 39-43); regarding claim 11, the determining means comprises a first counter for counting clock cycles of the input signal clock (Fig. 5, communication device, see "counter 43" recited in column 7 lines 10-16), , a second counter for counting cycles of the output signal clock (Fig. 5, communication device, see "counter 43" recited in column 7 lines 17-25) and means for simultaneously reading the counts of the first and second counters (Fig. 5, communication devices 11 and 12, see "selector 102" recited in column 8 lines 17-22 and lines 39-43); regarding claim 12, comprising a latch for storing the count of the counter counting the higher frequency clock (Fig.4, node distribution, see "latch for store" recited in column 6 lines 30-33) and the count being clocked into the latch by an edge of the lower frequency clock (Fig.4, node distribution, see "latch for store" recited in column 6 lines 36-39); regarding claim 16,) comprises the steps of applying the input clock of a module to a first counter within the module (Fig. 5, communication device, see "counter 43" recited in column 7 lines 10-16), applying the output clock of the module to a second counter within the module (Fig. 5, communication device, see

"counter 43" recited in column 7 lines 17-25) and reading the counts of the first and second counters simultaneously at given intervals (Fig. 5, communication devices 11 and 12, see "selector 102" recited in column 8 lines 17-22 and lines 39-43).

Hayashi et al. does not disclose the following features: regarding claim 1, a packet switched communications system for transmitting synchronous data from a source module to a terminating module and each module operating with a clock of nominal frequency but which is not synchronized with the clocks of the other module(s); regarding claim 2, in an ATM data cell; regarding claim 6, a method of recovering clock signals in a packet switched communications network and module operating with a clock of nominal frequency but which is not synchronized with the clocks of the other module(s) and regarding claim 7, the network uses asynchronous transfer mode (ATM) and in an ATM cell.

Eng et al. discloses a method of synchronizing the communication system with the following features: regarding claim 1, a packet switched communications system for transmitting synchronous data from a source module to a terminating module (Fig. 1, schematic diagram of the system, see "transmitting and receiving data" recited in column 1 lines 14-15 in the background of the invention) and each module operating with a clock of nominal frequency but which is not synchronized with the clocks of the other module(s) (Fig. 1, schematic diagram of the system, see "system based on own system clock" recited in column 1 lines 20-23 in the background of the invention); regarding claim 2, in an ATM data cell (Fig. 3, asynchronous network, see "ATM cell is transmitted" recited in column 4 lines 35-39); regarding claim 6, a method of recovering

clock signals in a packet switched communications network (Fig. 3, asynchronous network/IP-network, see "synchronizing with far end" recited in column 4 lines 35-39) and module operating with a clock of nominal frequency but which is not synchronized with the clocks of the other module(s) (Fig. 3, asynchronous network, see "system A and system B can not be synchronized" recited in column 4 lines 13-18) and regarding claim 7, the network uses asynchronous transfer mode (ATM) (Fig. 3, asynchronous network, see "ATM cell is transmitted" recited in column 4 lines 35-39) and in an ATM cell (Fig. 3, asynchronous network, see "ATM cell is transmitted" recited in column 4 lines 35-39).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Hayashi et al. by using the features, as taught by Eng et al. in order to provide the synchronization between the end nodes by transmitting the clock phase difference data via ATM cells. The motivation of transmitting the phase difference data via ATM cells is to enhance the functionalities of network to transport the phase difference data in real time in a cost effective manner.

6. Claim 5, 9-10, 13-15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (USP 5,062,124) in view of Eng et al. (USP 6,791,987 B1) as applied to claims1 and 8 above, and further in view of Rokugo (USP 5,864,248).

Hayashi et al. and Eng et al. describes the claimed limitations as discussed in

paragraph 5 above. Hayashi et al. discloses the following features: regarding claim 5, the means for transmitting the phase difference comprises (Fig. 2, synchronizing communication devices, see "transmitting the phase difference" recited in column 4 lines 14-25); regarding claim 13, the means for transmitting the phase difference comprises (Fig. 2, synchronizing communication devices, see "transmitting the phase difference" recited in column 4 lines 14-25); regarding claim 14, the means for transmitting the phase difference comprises (Fig. 2, synchronizing communication devices, see "transmitting the phase difference" recited in column 4 lines 14-25) and regarding claim 15, the means for transmitting the phase difference comprises (Fig. 2, synchronizing communication devices, see "transmitting the phase difference" recited in column 4 lines 14-25).

Hayashi et al. and Eng et al. do not disclose the following features: regarding claim 5, means for assembling an ATM cell containing the counts of the first and second counters; regarding claim 9, in which step d) comprises transmitting the counts read in step f; regarding claim 10, or in which the counters are read on a transition of the lower frequency clock; regarding claim 13, means for assembling an ATM cell containing the counts of the first and second counters; regarding claim 14, means for assembling an ATM cell containing the counts of the first and second counters and regarding claim 15, means for assembling an ATM cell containing the counts of the first and second counters; regarding claim 17, in which step d) comprises transmitting the counts read in step f); regarding claim 18, in which the counters are read on a transition of the lower frequency clock; regarding claim 19, in which the counters are read on a transition of

the lower frequency clock and regarding claim 20, in which the counters are read on a transition of the lower frequency clock.

Rokugo discloses phase-locked loop circuit (PLL) for producing clock signals synchronized with transmitter in receiver with the following features: regarding claim 5, means for assembling an ATM cell containing the counts of the first and second counters (Fig. 9, phase synchronization system, see "time data 93" recited in column 1 lines 40-49); regarding claim 9, in which step d) comprises transmitting the counts read in step f (Fig. 1, phase locked loop circuit, see "count value output from transmitter" recited in column 2 lines 22-40); regarding claim 10, or in which the counters are read on a transition of the lower frequency clock (Fig. 8, frequency response, see "data count value" recited in column 8, lines 46-52); regarding claim 13, means for assembling an ATM cell containing the counts of the first and second counters (Fig. 9, phase synchronization system, see "time data 93" recited in column 1 lines 40-49); regarding claim 14, means for assembling an ATM cell containing the counts of the first and second counters (Fig. 9, phase synchronization system, see "time data 93" recited in column 1 lines 40-49) and regarding claim 15, means for assembling an ATM cell containing the counts of the first and second counters (Fig. 9, phase synchronization system, see "time data 93" recited in column 1 lines 40-49) regarding claim 17, in which step d) comprises transmitting the counts read in step f) (Fig. 1, phase locked loop circuit, see "count value output from transmitter" recited in column 2 lines 22-40); regarding claim 18, in which the counters are read on a transition of the lower frequency clock (Fig. 1, phase locked loop circuit, see "count value output from transmitter" recited

in column 2 lines 22-40); regarding claim 19, in which the counters are read on a transition of the lower frequency clock (Fig. 1, phase locked loop circuit, see "count value output from transmitter" recited in column 2 lines 22-40) and regarding claim 20, in which the counters are read on a transition of the lower frequency clock (Fig. 1, phase locked loop circuit, see "count value output from transmitter" recited in column 2 lines 22-40).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Hayashi et al. with Eng et al. by using the features, as taught by Rakugo, in order to provide the synchronization between the end nodes by transmitting the clock phase difference data via ATM cells. The motivation of transmitting the phase difference data via ATM cells is to enhance the functionalities of network to transport the phase difference data in real time in a cost effective manner.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. USP 5,140,611 (Jones et al.), USP 6,049,886 (Motoyama), USP 6,272,138 B1 (Weon), USP 6,661,811 B1 (Baker), USP 5,099,477 (Taniguchi et al.), USP 5,615,177 (Yahata), USP 6,021,128 (Hosoya et al.), USP 6,222,894 (Lee), USP 6,577,693 B1 (Wolf) and USP 6,735,711 B2 (Lutz).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed Bokhari whose telephone number is (571) 270-

3115. The examiner can normally be reached on Monday through Friday 8:00-17:00 Hrs..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang B. Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KWANG BIN YAO
SUPERVISORY PATENT EXAMINER